REMARKS

Summary of the Office Action

Claims 1, 5, 57 and 59 have been considered in the Office Action.

Claims 1, 5, 57 and 59 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office action asserts that the claim scope is uncertain because the claims include the trademark/trade name "VERILOG."

Claims 1, 5, 57 and 59 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Joe LoCicero and Donald E. Thomas, "A Multiheaded Multiple-Language Hardware/Software Cosimulator," 1997, Carnegie Mellon University, Research Report No. CMUCAD-97-34 ("LoC1997").

Reply to § 112, Second Paragraph Rejections

Claims 1, 5, 57 and 59 have been rejected under § 112, second paragraph, as being indefinite because the claims include the trademark/trade name "VERILOG." In particular, the Office action states that "the trademark/trade name is used to identify/describe a particular simulation environment, and accordingly, the identification/description is indefinite." Further, the Office action states that this § 112, second paragraph, rejection was first raised in the 13 September 2002 Office action, and that applicants cancelled each claim containing the VERILOG trademark to overcome the rejection.

First, the 13 September 2002 Office action included numerous claim rejections based on § 112, first and second paragraph. Of those rejections, the Office action rejected claims 4, 13-15, 18-20, 24, 26, 28, 34, 41-43, 46-48 and 51 based on § 112, second paragraph, because these claims included the trademark/trade name "VERILOG." To help advance prosecution of this application, applicants replied to the § 112, first and second paragraph, rejections by cancelling claims 2-4 and 6-54 without prejudice. Applicants never acknowledged or conceded the validity of the Examiner's specific assertion that claims including the term "VERILOG" are somehow indefinite.

Second, applicants expressly disagree that claims including the term "VERILOG" are indefinite. Indeed, as of today's date, the U.S. Patent and Trademark Office ("PTO") has issued 114 patents[1] that include the trademark/trade name "VERILOG." Included in this list, Ma U.S. Patent No. 6,957,423 ("Ma"), includes several claims that contain the trademark/trade name "VERILOG." The Ma patent issued from U.S. Patent Application Serial No. 09/858,764 ("the '764 application"), which was examined by the same Examiner as this application. Thus, the Examiner not only seemingly concluded that claims in the '764 application containing the trademark/trade name VERILOG were sufficiently definite, but he also expressly stated during prosecution of the '764 application that the VERILOG language was a "well-known circuit design language[]." Applicants respectfully agree with the Examiner that what was apparently well-known and sufficiently definite for the Ma patent is similarly well-known and definite for this application.

Independent claims 1 and 59 recite methods that include providing a single executable program adapted to create a primary thread and one or more secondary threads, the primary thread running VERILOG code on a VERILOG simulator. VERILOG code is code in a VERILOG language, which the Examiner himself declared to be "well known." A VERILOG simulator is a simulator that runs VERILOG code. Nothing in these claim terms is indefinite.

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[1] U.S. Patent Nos. 5,437,037, 5,537,580, 5,539,680, 5,764,951, 5,774,380, 5,794,072, 5,822,226, 5,850,348, 5,896,521, 5,903,475, 5,923,867, 5,937,190, 5,995,730, 6,012,033, 6,098,068, 6,108,678, 6,135,647, 6,148,316, 6,154,801, 6,161,211, 6,189,131, 6,195,539, 6,209,120, 6,223,142, 6,226,776, 6,226,780, 6,233,724, 6,247,165, 6,289,116, 6,304,837, 6,360,353, 6,401,230, 6,417,562, 6,442,738, 6,453,448, 6,466,898, 6,490,545, 6,493,852, 6,519,742, 6,532,554, 6,539,477, 6,539,520, 6,539,523, 6,557,147, 6,564,354, 6,571,375, 6,580,299, 6,594,816, 6,598,066, 6,606,734, 6,609,229, 6,618,838, 6,622,291, 6,625,798, 6,629,294, 6,634,012, 6,640,321, 6,643,617, 6,647,541, 6,651,228, 6,658,628, 6,658,630, 6,668,359, 6,684,381, 6,721,925, 6,735,743, 6,754,771, 6,759,898, 6,763,418, 6,782,511, 6,789,249, 6,792,579, 6,839,794, 6,871,172, 6,874,134, 6,877,139, 6,883,151, 6,895,367, 6,898,253, 6,898,767, 6,901,055, 6,904,577, 6,941,499, 6,948,139, 6,957,403, 6,957,423, 6,961,690, 6,973,631, 6,981,232, 6,983,234, 6,983,427, 6,985,842, 6,990,641, 7,007,248, 7,007,264, 7,016,996, 7,017,140, 7,020,140, 7,020,716, 7,036,114, 7,043,596, 7,047,173, 7,051,303, 7,051,304, 7,054,330, 7,058,053, 7,062,418, 7,062,425, 7,069,526, 7,080,365, 7,089,380, 7,092,360, 7,093,224, 7,100,133.

Accordingly, applicants respectfully submit that the claims in this case, like the claims in the 114 issued U.S. Patents that also include the term "VERILOG," are not indefinite. Accordingly, applicants respectfully request that the Examiner withdraw the § 112, second paragraph, rejections of claims 1, 5, 57 and 59.

Reply to § 102 Rejections

Claims 1, 5, 57 and 59 have been rejected under § 102(b) as being anticipated by LoC1997. The Examiner asserts that the simulation engine described in LoC1997 "may be considered a VERILOG simulator" because (1) "[t]he input to the [LoC1997] system is VERILOG source code, and the converted code, simulates identically to the original Verilog source code;" and (2) "[i]t is clear from the disclosure of [LoC1997] that VERILOG code is inputted to the system and simulated, along with all of its VERILOG-specific functionality." These assertions would be meaningful if they were actually relevant to the claimed invention. They are not.

Indeed, the Examiner seems to ignore the actual claim language. It is irrelevant that LoC1997's converted code "simulates identically to the original Verilog source code." The claims require providing a single executable program adapted to create a primary thread running VERILOG code. LoC1997 does not describe or suggest such a step, and instead expressly points away from it by describing a system that implements a simulator that runs C++ code, not VERILOG code.

Further, it is irrelevant that "VERILOG code is inputted to the system and simulated." This application does not merely claim inputting VERILOG code into a system and simulating it. The application actually claims methods that include providing a single executable program adapted to create a primary thread and one or more secondary threads, the primary thread running VERILOG code on a VERILOG simulator. LoC1997 does not describe such methods, regardless of the Examiner's strained assertions to the contrary.

Conclusion

Applicants seek an end to the seemingly interminable prosecution of this application. For the reasons stated above, applicants respectfully submit that this

application, including claims 1, 5, 57 and 59, is allowable. Applicants therefore respectfully request that the Examiner allow this application.

Respectfully submitted,

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